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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,040	04/03/2001	Ichiro Kumata	SON-2065	8745

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EXAMINER	
NG, CHRISTINE Y	
ART UNIT	**PAPER NUMBER**
2663	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,040	KUMATA, ICHIRO	
	Examiner	Art Unit	
	Christine Ng	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 5, 9, 10, 11, 13, 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,994,946 to Zhang.

Referring to claims 1 and 16, Zhang discloses in Figure 2 a crosstalk cancellation circuit for suppressing crosstalk noise of interconnections in an integrated circuit comprising:

N (N is an even number of 2 or more: 2) number of first inverters (inverter 121 at point 201, inverter 122 at point 203). Refer to Column 4, lines 9-31.

A first interconnection (first transmission line 101) for connecting the N(2) number of first inverters in series. Refer to Column 4, lines 9-31.

N(2) number of second inverters (inverter 121 at point 202, inverter 122 at point 204). Refer to Column 4, lines 9-31.

A second interconnection (second transmission line 101) for connecting said N(2) number of second inverters in series. Refer to Column 4, lines 9-31.

Wherein said first and second interconnections are arranged adjacent in parallel or substantially parallel to each other. Refer to Column 4, lines 9-17.

Wherein at least one first inverter among said N number of first inverters is arranged at a location where crosstalk nose due to a parasitic capacity (capacitive coupling) between said first and second interconnections is canceled out or substantially canceled out on said second interconnection. "The balancing inverters 121 and the restoring inverters 122 are positioned on each transmission line 101 so as to minimize distances over which the first original signal 131 and the second original 132 are transmitted in parallel..." (Column 4, lines 12-15). Minimizing the distance over which the signals 131 and 132 are transmitted in parallel decreases crosstalk by minimizing the amount of delay when polarity changes. Refer to Column 3, line 44 to Column 4, line 6.

Wherein at least one second inverter among said N number of second inverters is arranged at a location where crosstalk nose due to a parasitic capacity (capacitive coupling) between said first and second interconnections is canceled out or substantially canceled out on said first interconnection. "The balancing inverters 121 and the restoring inverters 122 are positioned on each transmission line 101 so as to minimize distances over which the first original signal 131 and the second original 132 are transmitted in parallel..." (Column 4, lines 12-15). Minimizing the distance over which the signals 131 and 132 are transmitted in parallel decreases crosstalk by minimizing the amount of delay when polarity changes. Refer to Column 3, line 44 to Column 4, line 6.

Referring to claim 2, Zhang discloses in Figure 2:

Said N number of first inverters are arranged in the approximately same interval (20% of distance 112, 60% of distance 112) in said first interconnection. Refer to Column 4, lines 18-24.

Said N number of second inverters are arranged in said second interconnection at the middle positions (40% of distance 112, 80% of distance 112) where distances from the adjacent first inverters are equal (inverters are 0.2 apart on alternating transmission lines). Refer to Column 4, lines 25-31.

Referring to claims 4 and 13, Zhang discloses in Figure 2 that said N number of first and second inverters and said first and second interconnections comprise buses (transmission lines 101) in said integrated circuit. Refer to Column 2, lines 37-39.

Referring to claims 5 and 15, Zhang discloses in Figure 2 that said N number of first and second inverters are inverters having the same configuration. All inverters invert the incoming signal. Refer to Column 3, lines 11-18.

Referring to claim 9, Zhang discloses in Figure 2 a method of interconnection of an automatic interconnection apparatus for laying out interconnections in an integrated circuit, comprising the steps of:

A first step of arranging a plurality of interconnections (first and second transmission lines 101) parallel or substantially parallel. Refer to Column 4, lines 9-31.

A second step of inserting the same number(2) of inverters at said plurality of interconnections (inverter 121 at point 201 and inverter 122 at point 203 on first transmission line 101; inverter 121 at point 202 and inverter 122 at point 204 on second transmission line 101). Refer to Column 4, lines 9-31.

Wherein said second step having a third step of inserting each inverter at a location where crosstalk noise due to a parasitic capacity (capacitive coupling) of the adjoining interconnections is canceled out or substantially canceled out on the related adjoining interconnections. Refer to the rejection of claim 1.

Referring to claim 10, Zhang discloses in Figure 2 that in said third step, inverters are inserted at alternate locations with respect to the interconnection adjoining each other among said plurality of interconnections. Each inverter is 0.2 apart on alternating transmission lines 101. Refer to Column 4, lines 18-31.

Referring to claim 11, Zhang discloses in Figure 2 that each inverter is inserted at one interconnection between interconnections adjoining each other at a location where the distance from the inverter of the other interconnection becomes the maximum (none) or in the vicinity (0.2) of that location. Each inverter is 0.2 apart on alternating transmission lines 101. Refer to Column 4, lines 9-31.

3. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,994,946 to Zhang in view of U.S. Patent No. 4,695,748 to Kumamoto.

Zhang et al do not disclose in each of said N number of first inverters, a time when an input signal voltage of the related first inverter changes and a time when an output signal voltage changes overlap, and in each of said N number of second inverters, a time when the input signal voltage of the related second inverter changes and a time when the output signal voltage changes overlap.

Kumamoto disclose in Figures 2-4 the input and output characteristics of an

inverter. In Figure 2, a change in the input voltage appears as a gradual change in the output voltage of the inverter. In Figure 3, a minor change in the input voltage causes a large change in the output voltage of the inverter. Refer to Column 5, lines 8-19 and lines 40-60. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in each of said N number of inverters, a time when an input signal voltage of the related inverter changes and a time when an output signal voltage changes overlap, the motivation being that the input and output voltages of the inverter are related.

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,994,946 to Zhang in view of U.S. Patent No. 5,930,612 to Ito.

Zhang does not disclose that the integrated circuit is configured as a semiconductor integrated circuit manufactured by a process rule of less than 0.25 micrometers.

Ito discloses that "As semiconductor integrated circuits are constantly being reduced in sizes and increasing densities, the design rule is also gradually becoming small, and it will be soon on the order of quarter micrometer..." (Column 1, lines 13-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the integrated circuit is configured as a semiconductor integrated circuit manufactured by a process rule of less than 0.25 micrometers, the motivation being to reduce the size of the circuit in order to make the device more compact.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,994,946 to Zhang in view of U.S. Patent No. 4,916,337 to Leung et al.

Referring to claim 6, Zhang discloses in Figure 2 an interconnection module in an integrated circuit, comprising:

M (M is a natural number: 4) number of inverters (inverter 121 at point 201 or 202, inverter 122 at point 203 or 204). Refer to Column 4, lines 9-31.

Input lines of said M number of inverters (connected to input end of inverters).

Output lines of said M number of inverters (connected to output end of inverters).

L number of signal lines (transmission line 101 segments between inverters). Refer to Column 4, lines 9-31.

Wherein said input lines, said output lines, and said signal lines are parallel or substantially parallel to each other (transmission lines 101 connecting inverters are parallel to one another), and wherein said inverters, input lines, and output lines of the related inverters and said signal lines are alternately arranged (inverters are 0.2 apart on alternating transmission lines 101) (note, where M=1, L=M or L=M+1 and where $M \geq 2$, L=M, L=M+1, or L=M-1). In Figure 2, $M(4) \geq 2$, L(4) =M(4). Refer to Column 4, lines 9-31.

Zhang does not disclose input lines of said M number of inverters and output lines of said M number of inverters.

Leung et al disclose in Figure 1 an inverter with an input line 20 and an output line 22. Refer to Column 1, lines 12-28. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include input lines of said M number of inverters and output lines of said M number of inverters, the motivation being so that the inverter can be connected in circuitry to accept data as input, invert the data, and output the data as output.

Referring to claim 7, Zhang disclose in Figure 2:

M is an integer of 2 or more (4). Refer to Column 4, lines 9-31.

Said M number of inverters are arranged so as to be parallel in a direction vertical or substantially vertical to the direction of said signal lines. Refer to Column 4, lines 9-31.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,994,946 to Zhang in view of U.S. Patent No. 4,916,337 to Leung et al, and in further view of U.S. Patent No. 5,930,612 to Ito. Refer to the rejection of claim 14.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Ng whose telephone number is (571) 272-3124. The examiner can normally be reached on M-F; 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Ng
April 12, 2005

RICKY NGO
PRIMARY EXAMINER 4/14/05